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H1R RAA RAC
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(54) **Carrier substrate for electrical circuit element**

(57) A carrier substrate comprises an insulator base (6) with terminals (10–13) for external connection and a wiring portion (4) provided on the insulator base for connecting circuit elements to be mounted on the base to the terminals for external connection. The wiring portion includes a plurality of insulating films (9a, 9b, 9c), an electrode layer provided on the uppermost insulating layer (3a) for connection with the circuit elements, and conductors (5a) provided on the other insulating layers for connecting the electrode layer to the terminals for external connection. A circuit element (1) layer may further be provided on an insulating layer other than the uppermost insulating layer. The circuit element layer has circuit elements formed in a thin film. Alternatively or in addition to the circuit element layer, a wiring layer may further be provided.

FIG. 1

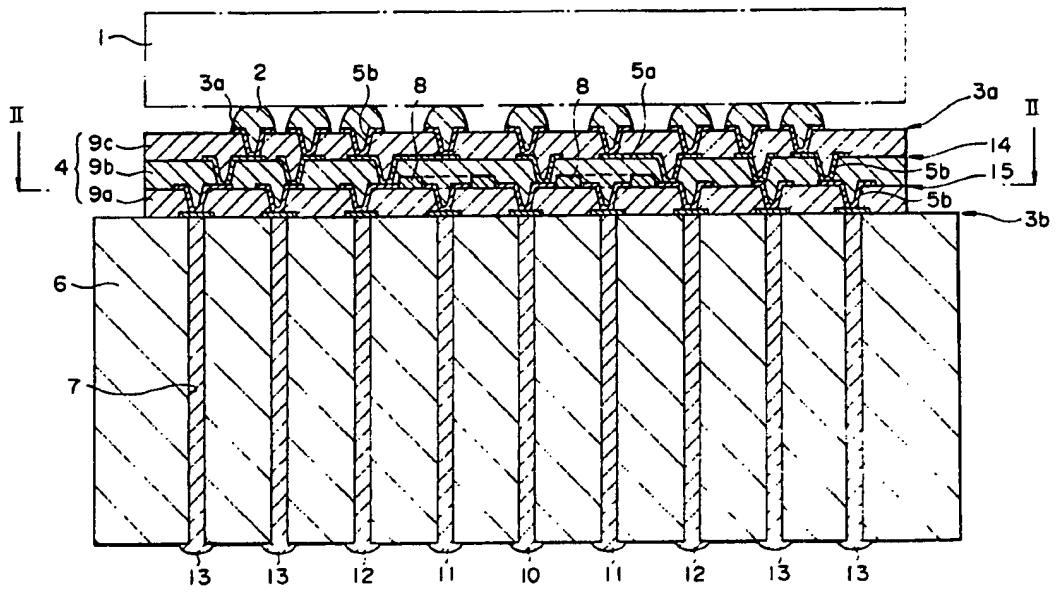


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FIG. 1

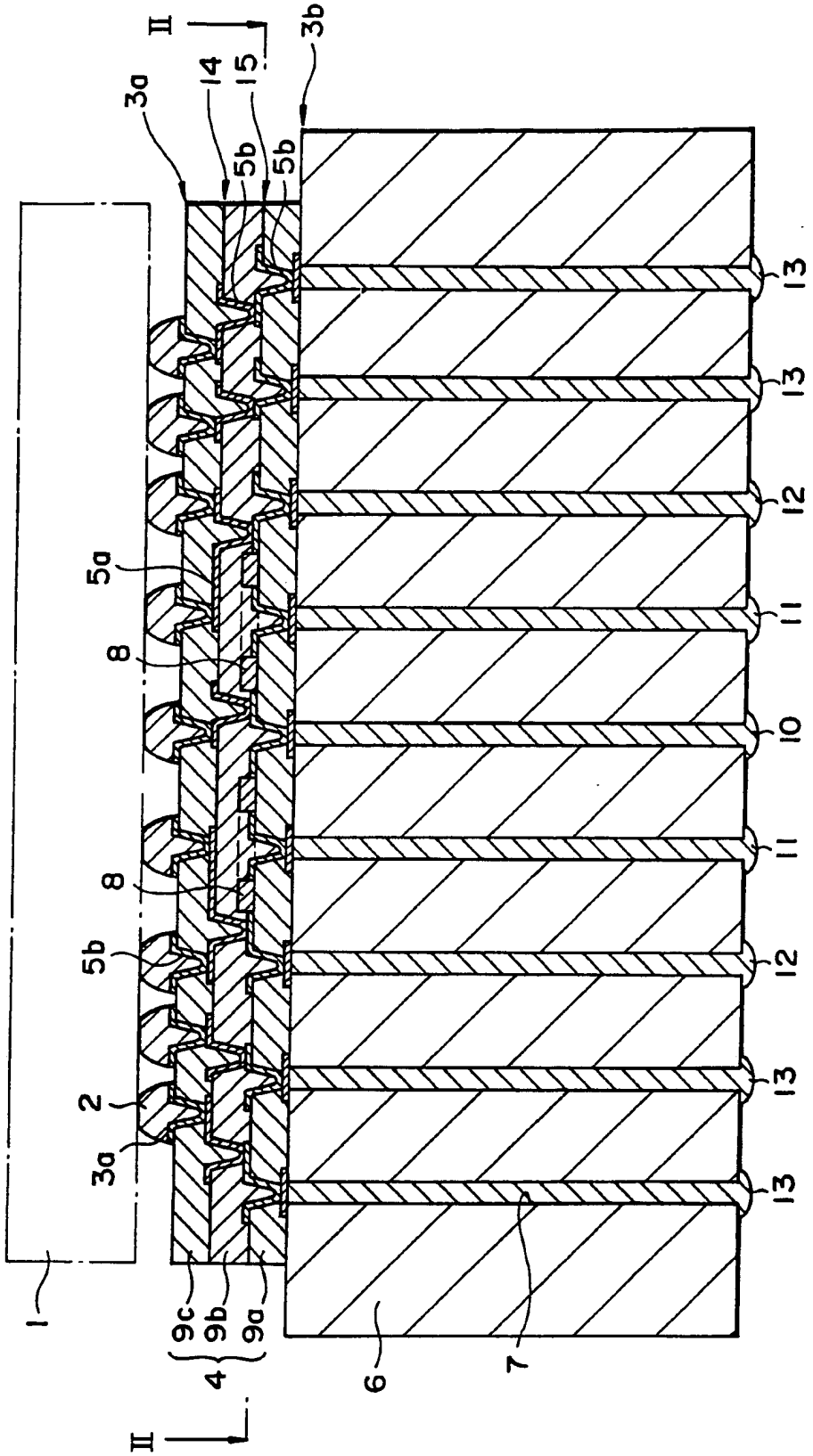
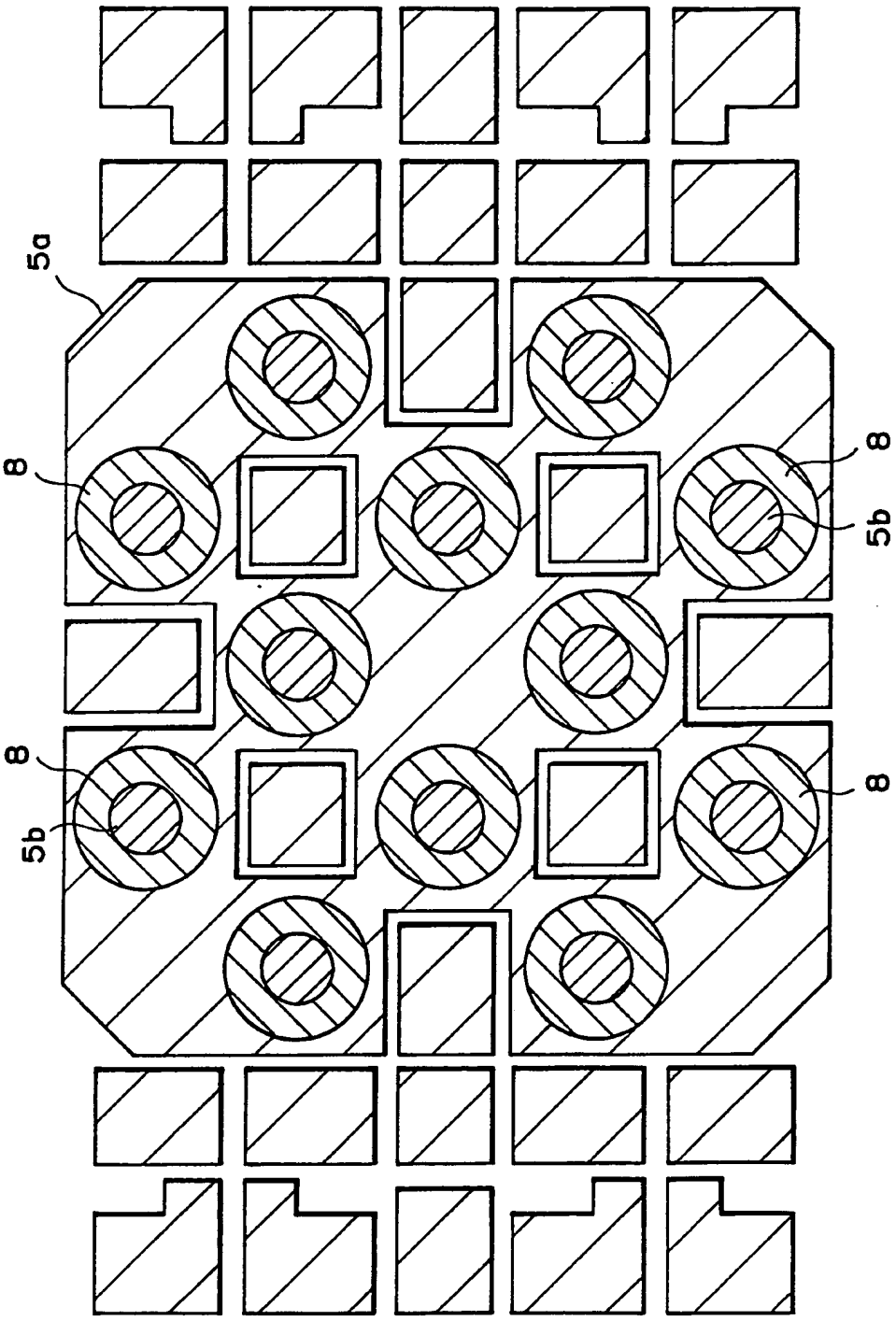

II
3b
14
15
3a
5b
5b
13
13
12
5a
11
8
10
11
8
5b
12
13
2
13
3a
1
9c
9b
9a
4
6
7
II

FIG. 2



# CARRIER SUBSTRATE AND METHOD FOR PREPARING THE SAME

This invention generally relates to a circuit element package, and more particularly relates to a carrier substrate for the circuit element package and a method for preparing the same, which is suitable for packaging a large scale integrated circuit such as a semiconductor integrated circuit.

Recently, circuits, especially semiconductor circuits are packaged in a package more and more at a higher density and integrated more and more, requiring increased number of pins available externally. To meet these requirements, a flip-chip bonding method has been proposed for the semiconductor integrated circuits, in which terminals are provided on every face of a chip instead of providing terminals only on the peripheral faces of the chip as had been done before. To cope this technique, terminals of the semiconductor package including such semiconductor integrated circuits are led out in grid, accordingly.

The semiconductor package of the type as referred to above generally comprises circuit elements such as semiconductor chips and a carrier substrate on which the semiconductor chips are mounted. The carrier substrate employed in the semiconductor package is generally a ceramic substrate which is made from metals of a

high melting point which are baked simultaneously.

On the other hand, a matched termination system is employed for circuits connected with a computer system. In the matched termination system, a transmission line is terminated in a resistance equal to the characteristic impedance of the line, so that there are no reflections and no standing waves.

For this reason, terminating resistances are put on around the package of the semiconductor integrated circuit or the chip to effect termination of the transmission lines when the semiconductor integrated circuit are mounted on the substrate.

The terminating resistors heretofore employed are discrete resistance chips. This imposes serious limitation on the size reduction task of the semiconductor integrated circuit package because such discrete resistance chips themselves have a limitation of small-sization and require substantial areas or spaces to be mounted on. Thus, the discrete resistance chips are not quite suitable for attaining increased packaging density. In other words, only a limited number of semiconductor integrated circuit packages or chips can be assembled to a circuit board as far as the discrete resistance chips are employed.

To solve this problem, a technique which is related to terminating resistance chips, but is capable of assembling an increased number of LSIs, is disclosed in Japanese Patent Un-examined Publication (KOKAI) No. 58-199552.

More particularly, this publication discloses a resistance chip comprising an insulator base and a plurality of resistance elements formed on the base, which is connected, at one end of the respective resistance element, to a through-hole connecting a

semiconductor chip and a circuit board and, at another end of the respective resistance element, to an electrode layer provided in the board. The resistance elements are formed on the insulator base such as a ceramic base by a thin-film forming technique or a thick-film forming technique and connected to the through-holes by wiring, respectively. The resistivities of the resistance elements are adjusted by laser trimming after the resistance elements have been prepared.

According to the technique disclosed in the publication, the resistance elements are preliminarily prepared as described above, and only the resistance elements which are needed for semiconductor chips and/or logical wirings provided on the board are left, removing the remaining resistance chips by cutting the wirings with laser beam. These resistance chips are connected to the semiconductor chips by soldering and the so formed assemblies are further connected to a board by soldering to be served for use.

This conventional art, however, fails to teach how to provide a number of resistance elements on the board. As described above, the resistivity of the resistance element such as a resistance module must be adjusted by trimming during manufacture. More specifically, in the case the resistance elements are provided as a thin film formed on a ceramic base, the resistivity of the film significantly varies locally due to roughness or irregularity of the surface of the ceramic base, which requires adjustment of resistivity. Whereas, in the case the resistance elements are provided in a thick film, accuracy of the resistivity can not be assured, which again requires adjustment of resistivity.

In this connection, it is to be noted that recent highly-integrated semiconductor circuit requires several

hundreds of or even more resistances and it is quite difficult to make adjustment for every resistances by measuring the respective resistivity and trimming the same.

Thus, the conventional technique as disclosed in the publication is not practical or even inpracticable in reality.

This conventional technique further fails to disclose desired arrangement of the resistances. More particularly, the resistances are provided adjacent to the through-holes which connect the circuit board to the semiconductor chips mounted thereon. Therefore, if the integration further increases and bumps are disposed more closely, the areas for mounting the resistances will be reduced. This will impose restriction on the size and arrangement of the resistances.

As can be seen from the foregoing, there is actually some difficulty to apply the technique as described above to a carrier substrate. Therefore, it is a task to solve the difficulty to realize a circuit package using the carrier substrate.

It is therefore an object of the present invention to provide a carrier substrate which is capable of providing thin-film circuit elements, for example, reistance elements with a reqired accuracy and a method for preparing the same.

It is another object of the present invention to provide a carrier substance and a method for preparing the same, which carrier substrate is capable of providing circuit elements such as resistance elements without substantial limitation of size and layout even when it is

required to mount a highly-integrated circuit elements in which bumps for connection are provided closely each other.

It is a further object of the present invention to provide a circuit element package using the carrier substrate as specified above.

To attain the objects as described above, there are provided three inventions for the carrier substrate.

A first invention features a carrier substrate comprising an insulator base with terminals for external connection and a wiring portion provided on the insulator base for connecting a circuit elements to be mounted on the carrier substrate with said terminals for external connection. The wiring portion includes a plurality of insulating films, an electrode layer provided on the uppermost insulating layer for connection with the circuit elements, a circuit element layer or layers provided on the insulating layer or layers other than the uppermost insulating layer and having circuit elements provided in the form of a thin film, and conductors provided on the insulating films for connecting the electrode layer to the terminal for external connection through the circuit element layer or layers.

A second invention features a carrier substrate comprising an insulator base with terminals for external connection and a wiring portion formed on the insulator base for connecting a circuit elements to be mounted on the carrier substrate to the terminal for external connection. The wiring portion includes a plurality of insulating films, an electrode layer provided on the uppermost insulating film and having electrodes for connection with the circuit elements, a wiring layer provided on any other insulating layer than the

uppermost insulating layer for coordinating the arrangement of the electrodes on the electrode layer with the terminals for external connection to connect the electrodes to the terminals, and conductors provided on the insulating layers for connecting the electrode layer to the terminals for external connection through the wiring layer.

A third invention features a carrier substrate comprising an insulator base with terminals for external connection and a wiring portion provided on the insulator base for connecting circuit elements to be mounted on the carrier substrate to the terminals for external connection; the wiring portion including a plurality of insulating films, an electrode layer provided on the uppermost insulating layer for connection with the circuit elements, a circuit element layer provided on the insulating layer other than the uppermost insulating layer and having circuit elements formed in a thin film, a wiring layer provided between the circuit element layer and the electrode layer for coordinating the arrangement of the electrodes on the electrode layer with the terminals for external connection to connect the electrodes to the terminals, and conductors provided on the insulating layers for connecting the electrode layer to the terminals for external connection through the wiring layer.

There is further provided a circuit element package wherein circuit elements are mounted on the carrier substrate as specified above for connection to the electrode layer of the carrier substrate.

There is still further provided a method for preparing a carrier substrate comprising an insulator base with terminals for external connection and a wiring portion provided on the insulator base for connecting

circuit elements to be mounted on the carrier substrate to the terminals of the insulator base for external connection, which method comprises the steps of: providing the wiring portions by forming an insulating film on the insulator base; forming circuit elements in a film on the insulating film; forming another insulating film on the film of the circuit elements; forming a wiring layer on said another insulating film for coordinating the circuit elements to be mounted on the carrier substrate with the external connection terminals of the insulator base for attaining connection therebetween; forming a further insulating film on the wiring layer; and forming an electrode layer on said further insulating film for connection with the circuit elements; and providing through-holes and wiring conductors in association with the respective insulating films.

In the carrier substrate according to the present invention, a ceramic base is preferably employed as the insulator base. The insulator base are provided with through-holes communicating with the upper and the lower surface of the base.

The thin-film circuit element may, for example, be a thin-film resistance element which may be used as a terminating resistance. The thin-film resistance element may be prepared by vacuum deposition with Cr cermet.

The insulating films are preferably made from organic materials such as polyimide.

The circuit element package according to the present invention is prepared preferably by mounting the circuit elements on the carrier substrate having the thin-film resistace elements. In this case, the the thin-film resistance elements may be used as terminating resistances.

The circuit elements to be assembled in the circuit

element package according to the present invention may be integrated circuits. Especially, a large scale integrated circuit such as a semiconductor LSI wherein elements are disposed at a high density may be suitably combined with the carrier substrate having a wiring layer.

According to the present invention, the insulating film is formed on the insulator base to form thin-film circuit elements such as thin-film resistance elements. Therefore, the irregularity or warp of the insulator base such as a ceramic base is levelled or evened by the insulating film provided under the thin-film circuit elements. Thus, the circuit elements can be free from undesired influences by the surface roughness of the insulator base. By this reason, circuit elements of a desired coefficient, for example, a resistivity can be prepared accurately. As a result of this, adjustment such as trimming is not needed any more for the circuit elements or thin-film resistance elements after they have been formed.

In the case the carrier substrate has a wiring layer on the insulating layer which connects, while coordinating, the electrode layer for connection with the circuits elements to be mounted on the carrier substrate with the terminals of the insulator base for external connection. Consequently, the terminals of the circuit elements to be mounted on the carrier substrate can be connected to the terminals of the insulator base for external connection even when the terminal layout of the circuit elements is not aligned with the terminal layout of the insulator base.

In addition, when the circuit elements to be mounted on the carrier substrate have terminal arrangement in which terminals are disposed very closely each other, the

terminal density of the terminal arrangement can be attained by the wiring layer. Consequently, when it is required to mount the circuit package which includes such circuit elements onto a printed circuit board, the connection operation can be handled more easily.

Furthermore, since the high-density terminal arrangement can be reduced to a lower-density terminal arrangement and the terminal arrangements can be coordinated with each other by the wiring layer, the signal or power supply positions can be changed freely, allowing the circuit designing to be more free. This makes the pattern or size of the circuit element formed on the circuit element layer can be determined more freely.

The present invention will now be described in greater detail by way of example with reference to the accompanying drawings, wherein:-

FIG. 1 is a sectional view showing one form of a carrier substrate according to the present invention and a circuit element package using the carrier substrate; and

FIG. 2 is a pattern diagram of conductor portions and resistor portions of the carrier substrate in section taken along a line II - II.

An embodiment of the present invention will now be described referring to the drawings.

FIG. 1 illustrates, in section, a configuration of the carrier substrate according to the embodiment.

The carrier substrate as illustrated comprises a ceramic base 6 and a thin-film wiring portion 4 provided on the ceramic base 6.

The ceramic base 6 is formed, for example, from ceramic powder containing alumina as a main material. The ceramic base 6 is formed with through-holes 7 and provided with terminals 10 to 13. The terminals 10 to 13 are to be used for connection when the ceramic base 6 is mounted to a printed circuit board (not shown). The ceramic base 6 may further be provided with a power supply layer or layers and/or a grounding layer or layers.

The terminal 10 is used as a common electrode terminal for resistance elements 8 which will be described in detail later. Each of the terminal 11 is used as an electrode terminal for the resistance element 8. The terminals 12 are general power supply terminals and the terminal 13 are general signal pins for a large scale integrated circuit (LSI) mounted on the carrier substrate. In the embodiment as illustrated, the terminal 10 is used as a specific power supply terminal for LSI as well as it is used as the electrode for the resistance element as mentioned above. Of course, separate terminals may be provided for these functions, respectively.

The thin-film wiring portion 4 is formed of insulation layers comprising insulating films 9a, 9b and 9c which are provided in this order from the bottom. A resistance layer 15 is provided between the insulating films 9a and 9b for forming the resistance elements 8. Similarly, a wiring layer 14 is provided between the insulating films 9b and 9c for forming conductor wiring 5a. On the top of the insulating film 9c is provided an upper connection layer 3a for connection with circuit elements which are to be mounted above the layer 3a. The insulating film 9a which forms the lowermost layer of the thin-film wiring portion 4 has, on the bottom surface thereof, a lower connection layer 3b formed at positions

corresponding to the terminals 10 to 13 of the ceramic base 6 for connection with these terminals 10 to 13, respectively.

The materials of the insulating films 9a, 9b and 9c are not critical and they may be made from any material so long as the material is capable of flushing or leveling the surface of the ceramic base 6. In the embodiment as being referred to, the insulating films 9a, 9b, 9c are made from an organic material such as polyimide resin. The materials of the respective layers may be different. However, the materials of these insulating layers 9a, 9b and 9c are preferably made of the same or similar materials to minimize a thermal stress which might be caused between the layers. The film on which the resistance layer is formed and which functions as a substrate for the resistance elements is preferably made from a material having a coefficient of thermal expansion similar to both the thermal expansion coefficient of the ceramic base and the thermal expansion coefficient of the resistance elements. Most preferably, a material having a coefficient of thermal expansion which is intermediate between the two thermal expansion coefficients.

The resistance layer 15, the wiring layer 14, the upper connection layer 3a and the lower connection layer 3b are connected with each other through the conductor wiring 5a and through-holes 5b and connected to the through-holes 7 of the ceramic base 6. The through-holes 5b are prepared by making holes in the insulating films 9a, 9b and 9c by etching and filling the holes with conductors.

The resistance elements 8 are formed by a thin film and they are formed in the shape of a ring as illustrated in FIG. 2. An inner periphery and an outer periphery of

the ring are connected to electrodes, respectively. Of course, the shape of the resistance elements 8 is not limited to the ring and they may be provided in another shape.

Although resistance elements 8 are provided as circuit elements in the embodiment as illustrated, another type of circuit elements may be provided alternatively or additionally. For example, capacitors may be provided. In the case where circuit elements such as terminating resistors are not required, the resistance elements 8 may be omitted.

FIG. 2 illustrates a plane of the resistance layer 15. As shown in the figure, the resistance layer 15 includes a plurality of resistance elements 8 and conductors 5a and through-holes 5b which also function as electrodes of the resistance elements 8.

In the embodiment as illustrated, one wiring layer 14 is provided as described before. This wiring layer 14 is provided for effecting adjustment with respect to differences in arrangements or layouts of terminals provided in the upper connection layer 3a which functions as an electrode layer for connection with circuit elements to be mounted above the connection layer 3a and the lower connection layer 3b to attain coordination between the upper connection layer 3a and the lower connection layer 3b. In the embodiment as illustrated, the wiring layer 14 enlarges the high-density terminal arrangement of the upper connection layer 3a into a terminal arrangement suited for the lower connection layer 3b. The wiring layer 14, therefore, may be omitted if there is no significant difference in terminal arrangement between the two connection layers. Or, a plurality of wiring layers may be provided according to necessity.

The wiring layer 14 is provided above the resistance layer 15 in the embodiment as illustrated.

The upper connection layer 3a has a terminal arrangement corresponding to an arrangement of bumps or balls provided on LSI 1 to be mounted on the wiring portion 4. The lower connection layer 3b has a terminal arrangement corresponding to an arrangement of the terminals 10 to 13 of the ceramic base 6.

The integrated circuit elements, i.e., LSI 1 is mounted on the thin-film wiring portion 4. LSI 1 is assembled with its bumps (not shown) placed on the terminals of the upper connection layer 3a, respectively, and bonded thereto by solder 2. Thus, a circuit element package or LSI package can be provided.

The configuration of the carrier substrate will now be described in detail, while referring to the method for fabricating the same.

The ceramic base 6 is prepared by a known method. For example, a dispersion or slurry of ceramic powder and liquid vehicle is prepared and cast into thin sheets by passing a leveling or doctor blade over the slurry. After drying, the sheets are cut to size, through-holes and cavities are mechanically punched, wiring paths are provided, and the through-holes are filled with metal. Several of these sheets are laminated and the entire structure is fired to form a monolithic sintered body for the ceramic base. In the course of the preparation process, the terminals 10 to 13 are formed on the ceramic base 6. The thin-film wiring portion 4 is provided on the ceramic base 6.

In the thin-film wiring portion 4, the lower connection layer 3b, the insulating film 9a, the resistance layer 15, the insulating film 9b, the wiring layer 14, the insulating film 9c and the upper connection

layer 3a are laminated in this order from the bottom.

The lower connection layer 3b is formed on the ceramic base 6 at positions corresponding to openings of the through-holes 7 which connect to the terminals 10 to 13, respectively. The layer 3b may be formed when the through-holes of the ceramic base 6 are filled with a conductive material.

The insulating films 9a, 9b and 9c are formed by coating a solution of varnish including polyimide, and drying and baking the same. Each of the insulating films 9a, 9b and 9c is provided with the conductors 5a and the through-holes 5b. The insulating films 9a, 9b and 9c are each subjected to etching to form holes or cavities therein and conductive materials are filled in the holes or cavities to form conductors 5a and through-holes 5b. The conductive materials are applied by metallizing or plating.

The insulating film 9a is first made. This insulating film 9a is formed as thick as it is capable of filling concaves or warp on the surface of the ceramic base 6 to form a smooth surface. It would suffice for the insulating film 9a to have a surface as smooth as the resistance elements 8 to be provided on the insulating film 9a is formed with a high accuracy. For example, the insulating film 9a is 10 to 30 μm thick.

On an upper surface of the insulating film 9a is provided the resistance layer 15. The resistance elements 8 are formed in this layer by a known method such as a vacuum deposition, sputtering, or the like. The resistance elements 8 are made from a resistive material such as Cr, Cr cermet, or the like. The resistance elements 8 are shaped in a desired pattern by applying vacuum deposition through a mask or applying photo-etching after deposition. The thickness of the

resistance element 8 is determined by a resistivity of the resistive material employed and a pattern of the resistance element formed. The thickness is for example 0.05 to 30 μm.

The insulating film 9b is formed on the resistance layer 15 in a manner as stated with reference to the film 9a.

The wiring layer 14 is provided on the insulating film 9b. The conductors 5a of the wiring layer 14 are made of aluminum. The conductors 5a of the wiring layer 14 are formed, for example, by vacuum deposition etc. in the same manner as described with reference to the resistance layer 15. In this step, a masking means may be used for obtaining desired wiring conductor patterns. Alternatively, a film of the conductor may be formed first, and then the patterns may be formed, for example, by photo-etching.

The insulating film 9c may be formed in a similar manner to that as described above after the wiring layer 14 has been formed.

The upper connection layer 3a is formed on the insulating film 9c. The conductors of the connection layer 3a are formed by the metal applied to the through-holes 5b formed between the wiring layer 14 and the upper connection layer 3a. Therefore, the conductors of the layer 3a can be formed simultaneously with the metal filling into the through-holes 5b. Alternatively, electrodes may be formed separately from the through-holes 5b and connected to the through-holes 5b.

The carrier substrate of the embodiment is thus prepared and LSI 1 may be mounted on the carrier substrate to provide an LSI package. For connection of LSI 1, solder balls 2 of a high melting point are applied to the upper connection layer 3a and LSI 1 is put on the

connection layer 3a with its bumps (not shown) placed on the corresponding solder balls 2, respectively, followed by melting the solder balls 2 to attain the desired connection.

The so prepared LSI package is mounted, for example, on a printed circuit board with the terminals 10 to 13 of the ceramic base 6 connected with the board by using solder having a melting point lower than that of the solder ball 2.

As described above, the insulating film 9a is provided on the ceramic base 6 and the resistance elements 8 are formed on the insulating film 9a. With this arrangement, the irregurality of the surface of the ceramic base 6 is evened by the insulating film 9a. As a result of this, the resistance elements 8 can be formed accurately.

The wiring layer 14 provided between the resistance layer 15 and the upper connection layer 3a presents the following advantageous effects.

First, it functions as an interface means for coordinating the terminal arrangement of the ceramic base and the terminal arrangement of the integrated circuit elements to be mounted on the ceramic base.

Secondly, the resistance elements can be free from restriction in position and area where the elements are provided, which restriction may possibly be caused in case leads of the terminals for the integrated circuit elements and the terminating resistance elements are present together. With this arrangement, a plurality of resistance elements may be provided in a desired arrangement and sizes without deteriorating the function of inputting and/or outputting with reference to the integrated circuit elements.

Thirdly, the terminal arrangement of the large

scale integrated circuit in which the terminals are provided at a high density is changed into the arrangement in which the terminals are provided at a reduced density due to the interface function of the wiring layer as described above. Consequently, the connection to the printed circuit board can be attained easily. In addition, since the size of the package itself becomes large, the handling of the package can be easier.

Although the invention has been described heretofore with reference to the carrier substrate for LSI and the LSI package employing the same as illustrated, the present invention is not limited to them.

The insulating films of the embodiment as given above are made of polyimide, but they may be made of another material, preferably an organic material.

Although both the resistance layer and the wiring layer are provided in the embodiment as illustrated, they are not necessarily needed when only the function of either one is required.

CLAIMS:-

1. A carrier substrate comprising an insulation base with terminals for external connection and a wiring portion provided on the insulator base for connecting a circuit elements to be mounted on the carrier substrate with said terminals for external connection;

said wiring portion including a plurality of insulating films, an electrode layer provided on the uppermost insulating layer for connection with the circuit elements, a circuit element layer or layers provided on the insulating layer or layers other than said uppermost insulating layer and having circuit elements formed in a thin film, and conductors provided on the insulating films for connecting said electrode layer to said terminal for external connection through said circuit element layer or layers.

2. A carrier substrate comprising an insulator base with terminals for external connection and a wiring portion formed on the insulator base for connecting a circuit elements to be mounted on the carrier substrate to the terminal for external connection;

said wiring portion including a plurality of insulating films, an electrode layer provided on the uppermost insulating film and having electrodes for connection with the circuit elements, a wiring layer provided on any other insulating layer than said uppermost insulating layer for coordinating the arrangement of the electrodes on the electrode layer with the terminals for external connection to connect the electrodes to the terminals, and conductors provided on the insulating layers for connecting the electrode layer

to the terminals for external connection through the wiring layer.

3. A carrier substrate comprising an insulator base with terminals for external connection and a wiring portion provided on the insulator base for connecting circuit elements to be mounted on the substrate to the terminals for external connection;

said wiring portion including a plurality of insulating films, an electrode layer provided on the uppermost insulating layer for connection with the circuit elements, a circuit element layer provided on the insulating layer other than said uppermost insulating layer and having circuit elements formed in a thin film, a wiring layer provided between the circuit element layer and the electrode layer for coordinating the arrangement of the electrodes on the electrode layer with the terminals for external connection to connect the electrodes to the terminals, and conductors provided on the insulating layers for connecting the electrode layer to the terminals for external connection through the wiring layer.

4. A circuit element package wherein circuit elements are mounted on the carrier substrate according to claim 1 for connection to the electrode layer of the carrier substrate.

5. A circuit element package wherein circuit elements are mounted on the carrier substrate according to claim 2 for connection to the electrode layer of the

carrier substrate.

6. A circuit element package wherein circuit elements are mounted on the carrier substrate according to claim 3 for connection to the electrode layer of the carrier substrate.

7. A carrier substrate according to claim 1, wherein the thin film circuit elements are thin film resistance elements.

8. A carrier substrate according to claim 3, wherein the thin film circuit elements are thin film resistance elements.

9. A circuit element package wherein said circuit elements are mounted on the carrier substrate according to claim 7 for connection to the electrode layer of the substrate.

10. A carrier substrate according to claim 1, wherein the insulating films are made of organic materials.

11. A carrier substrate according to claim 2, wherein the insulating films are made of organic materials.

12. A carrier substrate according to claim 3, wherein the insulating films are made of organic materials.

13. A method for preparing a carrier substrate comprising an insulator base with terminals for external connection and a wiring portion provided on the insulator base for connecting circuit elements to be mounted on the carrier substrate to the terminals of the insulator base for external connection, which method comprises the steps of:

providing the wiring portions by:

forming an insulating film on the insulator base;

forming circuit elements in a film on the insulating film;

forming another insulating film on the film of the circuit elements;

forming a wiring layer on said another insulating film for coordinating the circuit elements to be mounted on the carrier substrate with the external connection terminals of the insulator base for attaining connection therebetween;

forming a further insulating film on the wiring layer; and

forming an electrode layer on said further insulating film for connection with the circuit elements; and

providing through-holes and wiring conductors in association with the respective insulating films.

14. A carrier substrate constructed substantially as herein described with reference to and as illustrated in the accompanying drawings.

15. A method for preparing a carrier substrate substantially as herein described with reference to the accompanying drawings.

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